AMENDMENT TO THE CLAIMS

This listing of claims will replace all prior versions of claims in the application.

Listing of Claims:

1-22. (Canceled)

23. (New) An integrated circuit comprising:

a bus; and

a plurality of devices coupled to the bus in which individual devices include respective agents coupled to the bus to receive a clock signal having a rising edge and a falling edge, the agents to drive a signal onto the bus responsive to one of the rising or falling edge and to sample the signal on the bus responsive to other of the falling or rising edge to allow a signal to be driven by one agent and sampled by a second agent during one clock cycle.

24. The integrated circuit of claim 23, wherein the plurality of agents are disposed in the individual devices to perform as distributed agents in a distributed arbitration scheme.

25. The integrated circuit of claim 24, wherein the plurality of devices include a processor, cache memory, memory controller and input/output (I/O) interface, wherein agents within the processor, cache memory, memory controller and I/O interface drive and sample signals on the bus responsive to rising or falling edges of the clock signal.

26. The integrated circuit of claim 25, wherein an agent to request arbitration drives the bus with an arbitration signal responsive to the one of the rising or falling edge used to drive the bus and the arbitration signal is to be sampled responsive to the other of the falling or rising edge used to sample the bus, wherein the arbitration signal is to be evaluated during the one clock cycle to allow a winner of the arbitration to drive the bus on a next clock cycle on the one of the rising or falling edge used to drive the bus.

27. The integrated circuit of claim 25, wherein the agents to drive the bus responsive to the rising edge and to sample responsive to the falling edge.

28. The integrated circuit of claim 25, wherein the agents to drive the bus responsive to the falling edge and to sample responsive to the rising edge.

29. A method comprising:

driving a signal on a bus of an integrated circuit having a plurality of devices coupled to the bus, in which individual devices include respective agents coupled to the bus to receive a clock signal having a rising edge and a falling edge, wherein the signal is driven onto the bus responsive to one of the rising or falling edge; and

sampling the signal responsive to other of the falling or rising edge to allow a signal to be driven by one agent and sampled by a second agent during one clock cycle.

30. The method of claim 29, further comprising performing the driving and sampling on a plurality of agents that are distributed in a distributed arbitration scheme.

31. The method of claim 30, further comprising requesting arbitration by driving the bus with an arbitration signal responsive to the one of the rising or falling edge used for driving the bus and sampling the arbitration signal responsive to the other of the falling or rising edge used to sample the bus and evaluating the arbitration signal during the one clock cycle to allow a winner of the arbitration to drive the bus on a next clock cycle on the one of the rising or falling edge used for driving the bus.

32. The method of claim 30, wherein the driving is responsive to the rising edge and sampling is responsive to the falling edge.

33. The method of claim 30, wherein the driving is responsive to the falling edge and sampling is responsive to the rising edge.